AMENDMENTS TO THE SPECIFICATION:

Please amend the Specification at page 2, line 26, to page 4, line 18, as follows:

~~In order to achieve the objective, a pattern correcting method of a mask for manufacturing a semiconductor device comprising:~~

~~With the pattern correcting method of a mask for manufacturing a semiconductor device having the above constitution,~~

~~(1) As this method considers the relationship between a variation amount in line width of a line portion generated after wafer process and a space width from the portion where the line portion overlaps a contact portion to the portion another line portion adjoining this overlapped portion, that is, the environment around the pattern to be corrected is considered, sufficient correction accuracy can be obtained in comparison with a correcting method not considering the surrounding environment.~~

~~In connection with the surrounding environment, following environments can be considered:~~

~~(2) Relationship between a shortening amount of the line portion generated after the wafer process and the space width from the portion where the line portion overlaps the contact portion to another line portion adjoining this overlapped portion.~~

~~(3) Relationship between the shortening amount of the line portion generated after the wafer process and an area in a end portion of the line portion running across a transistor portion which is a gate end and not on the transistor portion.~~

~~(4) Relationship between a rounding amount on the transistor portion generated after the wafer process and the line portion.~~

~~(5) Relationship between the dimension of the line portion and a diameter difference between a first contact portion where the contact portion generated after the wafer process makes a contact with the transistor portion and a second contact portion where the contact portion makes a contact with the line portion.~~

~~(6) Relationship between the shortening amount of the line portion generated after the wafer process and the distance from the area where the line portion overlaps the contact portion to the end of the line portion.~~

~~(7) Relationship between the correction amount and the space width between one transistor portion and another adjoining transistor portion, if an enlarged contact portion adjoins one transistor portion or not.~~

A method is provided of pattern correcting a mask for manufacturing a semiconductor device. The method comprises extracting a correction portion to be corrected from a mask pattern on the mask, the correction portion being an overlapped portion where a line portion overlaps a contact portion. The method further comprises obtaining a surrounding environment of the correction portion, the surrounding environment of the correction portion being a space width between the line portion and another line portion. The method additionally comprises giving a variable correction amount to the correction portion in accordance with the surrounding environment, the variable correction amount being a line width given to the overlapped portion. The line width is increased by (i) an integer multiple of a design grid width in accordance with the space width and (ii) a misalignment amount.

In another aspect, a method is provided of pattern correcting a mask for manufacturing a semiconductor device. The method comprises extracting a correction portion to be corrected from a mask pattern on the mask, the correction portion being an overlapped portion where a line portion overlaps a contact portion. The method further comprises obtaining a surrounding environment of the correction portion, the surrounding environment of the correction portion being a space width between the line portion and another line portion. The method additionally comprises giving a variable correction amount to the correction portion in accordance with the surrounding environment, the variable correction amount being a line width given to the overlapped portion. The line width is increased by (i) an integer multiple of a design grid width in accordance with the space width, (ii) a misalignment amount, and (iii) half the design grid width.